EAST SEARCH

4/28/04

L#	Hits	Search String	Databases
L1	475	(vhdl or hdl) and (evolution$5 or genetic) and partition$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	38	1 and (partition$5 same (hardware and software))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	9	behavioral and genetic and (partition$5 same (hardware and software))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	54	1 and genetic and hardware and software	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Results of search set L2:

US 6668312 B2	System, method, and article of manufacture for dynamically profiling memory transfers in a program	20031223	711/170
US 6621298 B2	Variable grain architecture for FPGA integrated circuits	20030916	326/50
US 6389586 B1	Method and apparatus for invalid state detection	20020514	716/18
US 6380759 B1	Variable grain architecture for FPGA integrated circuits	20020430	326/41
US 6348813 B1	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	20020219	326/41
US 6333940 B1	Integrated digital loop carrier system with virtual tributary mapper circuit	20011225	370/506
US 6275064 B1	Symmetrical, extended and fast direct connections between variable grain blocks in FPGA integrated circuits	20010814	326/39
US 6216257 B1	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	20010410	716/16
US 6212566 B1	Interprocess communication protocol system modem	20010403	709/230
US 6211695 B1	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	20010403	326/40
US 6184713 B1	Scalable architecture for high density CPLDS having two-level hierarchy of routing resources	20010206	326/41
US 6181163 B1	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control signals	20010130	326/41
US 6150842 A	Variable grain architecture for FPGA integrated circuits	20001121	326/41
US 6130551 A	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	20001010	326/39
US 6127843 A	Dual port SRAM memory for run time use in FPGA integrated circuits	20001003	326/40

US 6107823 A	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	20000822	326/41
US 6097212 A	Variable grain architecture for FPGA integrated circuits	20000801	326/41
US 6081473 A	FPGA integrated circuit having embedded sram memory blocks each with statically and dynamically controllable read mode	20000627	365/230.01
US 6034544 A	Programmable input/output block (IOB) in FPGA integrated circuits	20000307	326/39
US 5990702 A	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VGBs) in FPGA integrated circuits	19991123	326/41
US 5982193 A	Input/output block (IOB) connections to MaxL lines, nor lines and dendrites in FPGA integrated circuits	19991109	326/39
US 5784377 A	Integrated digital loop carrier system with virtual tributary mapper circuit	19980721	370/463
US 20040073882 A1	Emulation solution for programmable instruction DSP	20040415	716/16
US 20040049609 A1	Mechanism for integrating programmable devices into software based frameworks for distributed computing	20040311	710/8
US 20040045015 A1	Common interface framework for developing field programmable device based applications independent of target circuit board	20040304	719/328
US 20040025133 A1	System and method for integrated circuit design	20040205	716/12
US 20030154465 A1	Method and system for verifying modules destined for generating circuits	20030814	717/137
US 20030154061 A1	Method for semi-automatic generation and behavioral comparison of models	20030814	703/4
US 20030149962 A1	Simulation of designs using programmable processors and electronically re-configurable logic arrays	20030807	717/135
US 20030140337 A1	System, method, and article of manufacture for data transfer reporting for an application	20030724	717/158
US 20030121010 A1	System, method, and article of manufacture for estimating a potential performance of a codesign from an executable specification	20030626	716/4
US 20030120872 A1	System, method, and article of manufacture for dynamically profiling memory transfers in a program	20030626	711/141
US 20030120460 A1	System, method, and article of manufacture for enhanced hardware model profiling	20030626	702/182
US 20030117971 A1	System, method, and article of manufacture for profiling an executable hardware model using calls to profiling functions	20030626	370/321
US 20030014611 A1	Software for designing, modelling or performing digital signal processing	20030116	712/35
US 20020186044 A1	Variable grain architecture for FPGA integrated circuits	20021212	326/41
US 20020100029 A1	System, method and article of manufacture for compiling and invoking C functions in hardware	20020725	717/140
US 20020072893 A1	System, method and article of manufacture for using a microprocessor emulation in a hardware application with non time-critical functions	20020613	703/26

Results of search set L4:

US 6668312 B2	System, method, and article of manufacture for dynamically profiling memory transfers in a program	20031223	711/170
US 6647358 B2	Pharmacokinetic-based drug design tool and method	20031111	703/2
US 6630351 B1	Compositions and methods for drug delivery using pH sensitive molecules	20031007	435/455
US 6609229 B1	Method for automatically generating checkers for finding functional defects in a description of a circuit	20030819	716/4
US 6578176 B1	Method and system for genetic algorithm based power optimization for integrated circuit designs	20030610	716/2
US 6557156 B1	Method of configuring FPGAS for dynamically reconfigurable computing	20030429	716/17
US 6551266 B1	Rheological treatment methods and related apheresis systems	20030422	604/6.09
US 6542858 B1	Pharmacokinetic-based drug design tool and method	20030401	703/2
US 6539532 B1	Method and apparatus for relocating elements in an evolvable configuration bitstream	20030325	716/16
US 6430736 B1	Method and apparatus for evolving configuration bitstreams	20020806	716/17
US 6407434 B1	Hexagonal architecture	20020618	257/401
US 6389586 B1	Method and apparatus for invalid state detection	20020514	716/18
US 6378122 B1	Method and apparatus for evolving a plurality of versions of a configuration bitstream in parallel	20020423	716/16
US 6363519 B1	Method and apparatus for testing evolvable configuration bitstreams	20020326	716/16
US 6363517 B1	Method and apparatus for remotely evolving configuration bitstreams	20020326	716/6
US 6360191 B1	Method and apparatus for automated design of complex structures using genetic programming	20020319	703/6
US 6312980 B1	Programmable triangular shaped device having variable gain	20011106	438/197
US 6097073 A	Triangular semiconductor or gate	20000801	257/401
US 6078736 A	Method of designing FPGAs for dynamically reconfigurable computing	20000620	716/16
US 5973376 A	Architecture having diamond shaped or parallelogram shaped cells	19991026	257/401
US 5889329 A	Tri-directional interconnect architecture for SRAM	19990330	257/758
US 5872380 A	Hexagonal sense cell architecture	19990216	257/369
US 5867397 A	Method and apparatus for automated design of complex structures using genetic programming	19990202	703/14
US 5864165 A	Triangular semiconductor NAND gate	19990126	257/401
US 5834821 A	Triangular semiconductor "AND" gate device	19981110	257/401
US 5822214 A	CAD for hexagonal architecture	19981013	716/10
US 5811863 A	Transistors having dynamically adjustable characteristics	19980922	257/401
US 5808330 A	Polydirectional non-orthoginal three layer interconnect architecture	19980915	257/208
US 5801422 A	Hexagonal SRAM architecture	19980901	257/369
US 5789770 A	Hexagonal architecture with triangular shaped cells	19980804	257/206
US 5777360 A	Hexagonal field programmable gate array architecture	19980707	257/315
US 5742086 A	Hexagonal DRAM array	19980421	257/300

US 5535342 A	Pld connector for module having configuration of either first PLD or second PLD and reconfigurable bus for communication of two different bus protocols	19960709	710/315
US 20040073534 A1	Method and apparatus for data mining to discover associations and covariances associated with data	20040415	707/1
US 20040058446 A1	Compositions and methods for drug delivery using pH sensitive molecules	20040325	435/455
US 20040048249 A1	Novel nucleic acids and secreted polypeptides	20040311	435/6
US 20040025133 A1	System and method for integrated circuit design	20040205	716/12
US 20030201933 A1	Low cost system and method for making dual band GPS measurements	20031030	342/357.12
US 20030199090 A1	Compositions and methods for drug delivery using pH sensitive molecules	20031023	435/455
US 20030174859 A1	Method and apparatus for content-based image copy detection	20030918	382/100
US 20030140337 A1	System, method, and article of manufacture for data transfer reporting for an application	20030724	717/158
US 20030127390 A1	Rheological treatment methods and related apheresis systems	20030710	210/646
US 20030121010 A1	System, method, and article of manufacture for estimating a potential performance of a codesign from an executable specification	20030626	716/4
US 20030120872 A1	System, method, and article of manufacture for dynamically profiling memory transfers in a program	20030626	711/141
US 20030120460 A1	System, method, and article of manufacture for enhanced hardware model profiling	20030626	702/182
US 20030117971 A1	System, method, and article of manufacture for profiling an executable hardware model using calls to profiling functions	20030626	370/321
US 20030040505 A1	Synthetic phospholipids to ameliorate atherosclerosis and other inflammatory conditions	20030227	514/78
US 20030018630 A1	Associative database scanning and information retrieval using FPGA devices	20030123	707/3
US 20030014611 A1	Software for designing, modelling or performing digital signal processing	20030116	712/35
US 20020142953 A1	Materials and methods relating to lipid metabolism	20021003	514/12
US 20020127623 A1	Biosensors, reagents and diagnostic applications of directed evolution	20020912	435/7.92
US 20020100029 A1	System, method and article of manufacture for compiling and invoking C functions in hardware	20020725	717/140
US 20020072893 A1	System, method and article of manufacture for using a microprocessor emulation in a hardware application with non time-critical functions	20020613	703/26
US 20010010091 A1	Method and apparatus for maximizing test coverage	20010726	716/4